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Voltage Compensation

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1 **TECHNICAL FIELD**

2 This invention relates to adjusting voltages used in circuits such as
3 integrated circuits.

5 **BACKGROUND**

6 As CMOS and other semiconductor technologies shrink in size, there are
7 corresponding improvements in device capacity, bandwidth, and cost. However,
8 shrinking process technologies also present challenges, often requiring designers
9 to compensate for various undesirable side-effects.

10 As an example, as semiconductor processing technologies have improved,
11 the interconnect traces that semiconductor devices manufacturers use to
12 interconnect components on integrated circuits have become much smaller in both
13 width and depth. Because of this, such traces are often more resistive than in the
14 past. Furthermore, smaller sizes and thinner oxide layers often increase the
15 current leakage of transistor gates. These two factors combine to produce higher
16 voltage drops along device interconnect traces. Such voltage drops can pose
17 problems in many situations, including for example, reduced voltage margins and
18 signal integrity.

19 The increased density of semiconductor devices also increases the coupling
20 of noise from adjacent traces and device elements.

21 Compounding these problems is the tendency of many newer devices to
22 utilize lower signal voltages. Voltage drop and noise coupling become even more
23 problematic in the face of such lower absolute and relative voltages.

24 Various forms of differential signaling are often used to address the
25 problems mentioned above. In one form of differential signaling, often referred to

1 as "pseudo-differential" signaling, a common reference voltage is distributed to
2 multiple signal receivers. Signal voltages are then specified relative to the
3 reference voltage.

4 To reduce the effects of voltage drop and noise coupling, both a signal and
5 its associated reference voltage are given similar physical routings. Because of
6 their similar routings, both the signal and the reference voltage are subject to
7 similar degrading influences (such as voltage drop and noise coupling), and the
8 signal voltage therefore maintains a generally fixed—or at least proportional—
9 relationship with the reference voltage.

10 Fig. 1 shows an example of a prior art circuit 10 using pseudo-differential
11 signaling. The circuit has a plurality of signal or data receivers 12, each of which
12 receives one of signals D_0 through D_3 . In addition, a common reference voltage
13 V_{ref} is distributed to each of receivers 12.

14 In a circuit such as this, the receivers 12 are often arranged in a star or
15 "Kelvin" configuration, in which the traces that distribute V_{ref} to each receiver are
16 approximately the same length. Furthermore, in many implementations the signals
17 D_0 through D_3 are routed so that they have similar lengths as the traces that
18 conduct V_{ref} , and are therefore subject to similar signal degradations such as noise
19 coupling and voltage drops.

20 The signals can be digital data signals or analog signals. In either case, the
21 receivers interpret the respective signals D_0 through D_3 by comparing them to the
22 reference voltage V_{ref} , and in response produce output signals O_0-O_3 .

23 The techniques illustrated in Fig. 1 are effective to some degree, but can be
24 insufficient in devices where interconnect resistances are high and/or where there
25 are large leakage currents. In Fig. 1, for example, trace resistance is represented

1 by discrete resistor elements R and leakage currents are represented by I. The
2 voltage drop over the length of the V_{ref} traces is equal to the product of I and R.
3 As an example, the traces of a modern CMOS process might exhibit a resistance
4 of 100 milli Ohms per square of trace length. Leakage currents might be on the
5 order of 200nA per squared micron. Assuming a trace length of 1000 microns and
6 a trace width of 0.33 microns, a typical interconnection scheme might produce a
7 voltage drop of approximately 192 mV between the nominal reference voltage and
8 the actual voltage as it is received by various components.

9 Such a drop in reference voltage V_{ref} can result in significantly decreased
10 margin or "headroom" between V_{ref} and ground: as V_{ref} approaches ground, there
11 is a smaller and smaller range of voltages that qualify as "low" in comparison to
12 V_{ref} . This has the effect of increasing the sensitivity of the circuit to noise. The
13 problem is particularly acute in high-speed devices where even the nominal or
14 ideal V_{ref} value is relatively low. In devices such as these, any further lowering of
15 V_{ref} threatens to significantly impair device operation. Furthermore, as
16 semiconductor process technologies continue to shrink and operating voltages
17 continue to decrease, voltage drops such as this will become even more
18 significant.

19

20 **BRIEF DESCRIPTION OF THE DRAWINGS**

21 Fig. 1 is block diagram showing distribution of a reference voltage in
22 accordance with the prior art.

23 Fig. 2 is a schematic view illustrating an embodiment of a circuit that
24 provides a compensated reference voltage.

1 Fig. 3 is a schematic view of a one embodiment of a reference voltage
2 driver such as used in the circuit of Fig. 2.

3 Fig. 4 is a schematic view of another embodiment of a reference voltage
4 driver such as used in the circuit of Fig. 2. Similar components in Figs. 4 and 3
5 are indicated by identical reference designators.

6 Fig. 5 is a schematic view of yet another embodiment of a reference voltage
7 driver such as used in the circuit of Fig. 2. Similar components in Figs. 5 and 3
8 are indicated by identical reference designators.
9

10 **DETAILED DESCRIPTION**

11 Fig. 2 shows pertinent components of an integrated circuit 100 that utilizes
12 voltage compensation. The integrated circuit can be implemented using
13 semiconductor processing technologies, including CMOS and bipolar processing
14 technologies, as well as by other present and future circuit technologies. The
15 present invention may also be implemented on printed circuit board (using for
16 example PCB fabrication technology), and/or using discrete devices.

17 As an example, integrated circuit 100 might comprise a memory device
18 having a plurality of memory storage cells and various control circuits to facilitate
19 writing to and reading from the storage cells. Various types of memory devices
20 might utilize the illustrated components or similar components that make use of
21 the illustrated principles, such as DRAM, EDO DRAM, SRAM, SDRAM, and
22 Rambus® DRAM. Many of these memory devices use differential and/or pseudo-
23 differential for internal and/or chip-to-chip data communications, and rely to
24 varying degrees on various types of voltages, including reference voltages, being
25 maintained within very close tolerances.

The integrated circuit of Fig. 2 includes one or more components 112 that operate with reference to a distributed reference voltage. In the described embodiment, components 112 comprise means for evaluating a plurality of data signals relative to a distributed reference voltage. More specifically, such means comprise a plurality of signal receivers, designated by reference numerals 112(a) through 112(d). The receivers are configured to evaluate corresponding signals D_a through D_d relative to a distributed reference voltage V_{dis} . Although four signals and four signal receivers are shown in Fig. 2, the present invention may be implemented with any number of signals and signal receivers.

In the described embodiment, the data signals are digital signals representing binary data such as memory read/write data, control data, address data, etc. In other embodiments components 112 might be configured to evaluate other types of signals, including analog signals.

Although the signal receivers shown in Fig. 2 can be of different types, the described embodiment utilizes differential data receivers, each of which compares two input voltages and produces a binary output signal as a function of which of the voltages is greater. The binary output signals are designated in Fig. 2 as O_a through O_d . In the configuration shown, one of the two inputs of a particular signal receiver 112 receives distributed reference voltage V_{dis} . The second of the two inputs is a data signal D , which is specified and evaluated relative to V_{dis} to represent a binary value. For example, a binary “1” might be represented by a data signal D that is greater than V_{dis} , while a binary “0” might be represented by a data signal D that is less than V_{dis} . The respective data signals are designated in Fig. 2 as D_a through D_d .

Integrated circuit 100 further comprises driver means having a variable voltage gain for producing a compensated reference voltage. Such driver means in the described embodiment comprise a reference voltage driver 114 that produces a compensated reference voltage V_{comp} . Routing means are provided for routing the compensated reference voltage V_{comp} on the integrated circuit to form the distributed reference voltage V_{dis} at receivers 112. Specifically, the compensated reference voltage V_{comp} is routed on the integrated circuit through traces to the individual data receivers 112, and forms V_{dis} at the receivers 112. Compensated reference voltage V_{comp} is subject to signal degradations such as noise coupling and voltage changes over the lengths of the traces. The degraded reference voltage is what is received by components 112(a) through 112(d); V_{dis} is a degraded or voltage-changed form of V_{comp} . Depending on the direction of current leakage, V_{dis} might be either higher or lower than V_{comp} . In a circuit where the input stages of components 112(a) through 112(d) sink current, the voltage degradation will normally correspond to a voltage drop relative to V_{comp} . In circuits where the input stages of components 112(a) through 112(d) source current, the voltage degradation will normally correspond to a voltage increase relative to V_{comp} .

More specifically, the distribution traces have finite resistances or impedances along their lengths that contribute to the degradation or voltage change of distributed reference voltage V_{dis} . Such resistances are represented in Fig. 2 by finite resistor elements R_a through R_d , although it should be recognized that the resistances are distributed along the lengths of the traces rather than being discrete elements. Furthermore, signal receivers 112 have input characteristics

1 that contribute to the degradation of distributed reference voltage V_{dis} . Such input
2 characteristics typically include finite input impedances and/or leakage currents.

3 Specifically, the signal receivers have leakage currents that are represented
4 in Fig. 2 by symbols I_a through I_d . It should be noted that although the noted
5 leakage currents typically result from input characteristics of receivers 112, such
6 as CMOS gate leakage, they could also be due to other factors. For example,
7 some circuits might utilize an input capacitance to reduce high-frequency noise or
8 to perform some other function. An input capacitance such as this can be an
9 additional source of leakage current. Furthermore, leakage currents I_a through I_d
10 might be either positive or negative. In a circuit implemented with bipolar
11 transistor technology, for example, a receiver input might comprise the base of a
12 bipolar transistor. If the transistor is an NPN transistor, there will normally be a
13 positive base current, into the receiver input. If the transistor is a PNP transistor,
14 however, the base will typically source a negative base current.

15 As discussed above in the “Background” section, trace resistances R_a
16 through R_d and leakage currents I_a through I_d can be a significant cause of
17 reference voltage signal degradation. Specifically, these factors cause a voltage
18 change in distributed reference voltage V_{dis} relative to compensated reference
19 voltage V_{comp} (either an increase or a decrease, depending on the directions of
20 leakage currents I_a through I_d). This voltage change is at least partially a function
21 of the lengths of the traces and the input characteristics of the receivers 112.

22 Compensated reference voltage V_{comp} is preferably distributed in a star,
23 Kelvin, length-matched, or impedance-matched configuration to approximately
24 equalize signal degradations in distributed reference voltage V_{dis} as it is received
25 by the various signal receivers. In addition, data signals D are typically routed in a

1 similar fashion as distributed reference voltage V_{dis} so that the data signals are
2 subject to approximately the same degradations as distributed reference voltage
3 V_{dis} .

4 Generally, the various signal paths to the inputs of receivers 112 are
5 designed to have matching impedances, to result in similar voltage degradations
6 over the lengths of the signal paths. In situations where the respective conductors
7 or traces that convey V_{dis} to the various signal receivers have approximately the
8 same physical and/or electrical characteristics (i.e., similar conductive metal,
9 width, and thickness), the conductors are simply length-matched to achieve such
10 impedance matching. In many cases, the signal paths or conductors will be
11 considered to be matched if their impedances fall within approximately 10% of
12 each other, although various circuits might require more or less matching
13 precision, depending on the nature of the circuits and process technologies
14 utilized. In some applications, it may be desirable to match impedances to within
15 1%.

16 Reference voltage driver 114 is responsive to feedback derived from
17 distributed reference voltage V_{dis} to adjust compensated reference voltage V_{comp} so
18 that V_{dis} is approximately equal to a nominal reference voltage V_{nom} . Such
19 feedback is produced by a feedback component 120. Feedback component 120
20 comprises feedback means for evaluating distributed reference voltage V_{dis} relative
21 to nominal reference voltage V_{nom} to derive or produce a feedback signal F.
22 Reference voltage driver 114 is responsive to feedback signal F to increase and
23 decrease compensated reference voltage V_{comp} as necessary to make distributed
24 reference voltage V_{dis} approximately equal to nominal reference voltage V_{nom} .

In the described embodiment, feedback component 120 is a receiver that is designed similarly to data signal receivers 112: as a signal comparator that compares two input voltages and produces a binary output depending on which of the input voltages is greater. As with data signal receivers 112, one of the inputs is configured to receive distributed reference voltage V_{dis} .

In a preferred embodiment, distributed reference voltage V_{dis} is provided to feedback receiver 120 in the same way it is provided to signal receivers 112, to result in similar degradations or voltage changes at the signal receivers 112 and the feedback receiver 120. That is, V_{comp} is distributed utilizing a star, Kelvin, length-matched, or impedance-matched physical routing to form V_{dis} at each of the data receivers 112 and at feedback receiver 120. In the situation where the conductors have similar physical and/or electrical characteristics (i.e., similar conductive metal, width, and thickness), the traces are similarly routed so that the trace lengths are approximately the same between each individual receiver (both data signal receivers 112 and feedback receiver 120) and reference voltage driver 114. More generally, the conductors or traces are impedance-matched to achieve similar voltage degradations or changes at the signal receivers 112 and the feedback receiver 120. Again, in many cases the impedances will be considered matched if they are within 10% of each other, although the matching precision will vary depending on the particular constraints and design goals of the circuit and the process technologies utilized in forming the conductors. In some applications, it may be desirable to match impedances to within 1%.

The trace impedance is represented in Fig. 2 as R_F . The desired result of the length-matched or impedance-matched routing is that all trace impedances, R_a , R_b , R_c , R_d , and R_F are approximately matched or equal, and that V_{dis} is subject to

1 approximately the same signal degradations as it is routed to both signal receivers
2 112 and feedback receiver 120.

3 Furthermore, feedback receiver 120 is designed and configured to have
4 similar input characteristics—specifically, a similar input impedance—as data
5 signal receivers 112, in order to contribute similar degradation or signal drop to
6 V_{dis} at feedback receiver 120. Because of this, feedback receiver 120 exhibits a
7 similar amount of input current leakage I_F as data signal receivers 112. That is, I_a ,
8 I_b , I_c , I_d , and I_F are all approximately equal (again, a 10% variance will usually be
9 considered to be approximately equal, although 1% may be desirable in certain
10 applications). This, in combination with the length-matched distribution of the
11 reference voltage, results in a voltage drop in V_{dis} relative to V_{comp} that is
12 approximately the same at feedback receiver 120 as it is at each of the data
13 receivers 112. Thus, V_{dis} is approximately the same (within 10%, or 1% for more
14 sensitive applications) at feedback receiver 120 and at each of data receivers 112.

15 The second input of feedback receiver 120 is configured to receive nominal
16 reference voltage V_{nom} . V_{nom} is the nominal or desired voltage of V_{dis} , and is
17 provided to feedback receiver 120 in a manner such that it is not subject to
18 significant voltage drop or other signal degradations. For instance, V_{nom} might be
19 distributed using a relatively short and/or wide trace to avoid a voltage drop.

20 Feedback receiver 120 may be configured so that it produces a feedback
21 signal F that is positive or logically true when V_{dis} is less than V_{nom} and negative
22 or logically false when V_{dis} is greater than V_{nom} . Reference voltage driver 114 is
23 configured to respond to feedback signal F by increasing compensated reference
24 voltage V_{comp} when signal F is true and decreasing compensated reference voltage
25 V_{comp} when signal F is false. The result is that V_{comp} is increased when $V_{dis} < V_{nom}$

1 and V_{comp} is decreased when $V_{dis} > V_{nom}$. This ensures that V_{dis} remains
2 approximately equal to V_{nom} . Alternatively, feedback receiver 120 may be
3 configured so that it produces a feedback signal F that is negative or logically false
4 when V_{dis} is less than V_{nom} and positive or logically true when V_{dis} is greater than
5 V_{nom} ; and driver 114 may be configured to respond to feedback signal F by
6 increasing compensated reference voltage V_{comp} when signal F is false and
7 decreasing V_{comp} when F is true.

8 Feedback receiver 120 optionally incorporates a low-pass filter after its
9 input stage, implemented in such a way that it does not significantly affect the
10 input characteristics of the feedback receiver. In a preferred embodiment, the low-
11 pass filter comprises a capacitor that is added to the receiver after its gain stage.
12 The capacitor works together with a resistive gain load to introduce a low-pass
13 filter effect without affecting the input stage.

14 Fig. 3 shows an exemplary implementation of reference voltage driver 114.
15 In this implementation, the voltage driver comprises an increment/decrement
16 component or up/down counter 130 and a variable gain amplifier 132. Generally,
17 up/down counter 130 is configured to increment and decrement a digital value 131
18 depending on the relationship of the distributed reference voltage V_{dis} and the
19 nominal reference voltage V_{nom} , as indicated by feedback signal F. Specifically,
20 counter 130 increments value 131 when $V_{dis} < V_{nom}$ and decreases value 131
21 when $V_{dis} > V_{nom}$. Even more specifically, up/down counter 130 has an up/down
22 or +/- input 133 that receives feedback signal F. When feedback signal F is
23 logically true, the counter periodically increments digital output value 131. When
24 feedback signal F is logically false, the counter periodically decrements digital
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1 output value 131. The output value 131 in this embodiment comprises a plurality
2 of individual bit lines.

3 Counter 130 functions as a means of controlling the voltage gain of driver
4 114. Output value 131 is supplied to variable gain amplifier 132, which has a
5 variable gain that is controlled or established by value 131: higher values cause
6 amplifier 132 to have a higher gain, while lower values cause amplifier 132 to
7 have a lower gain. Thus, the gain of amplifier 132 increases when $V_{dis} < V_{nom}$ and
8 decreases when $V_{dis} > V_{nom}$.

9 In the illustrated embodiment, variable gain amplifier 132 comprises an op-
10 amp 134 capable of sinking or sourcing current to provide positive or negative
11 amplification of nominal reference voltage V_{nom} . Op-amp 134 is biased by
12 resistors R_g , R_h , and R_{v1} . A first input of op-amp 134 receives V_{nom} through R_g .
13 A second input of amplifier 132 is connected to ground through R_h . The gain of
14 amplifier 132 is controlled by a digitally controllable variable resistor R_{v1} , which
15 is connected in series between the second input and the output of the op-amp 134.
16 In the described embodiment, R_g has half the resistance of R_h . R_h is equal to a
17 nominal or intermediate value within the range of resistances that can be produced
18 by variable resistor R_{v1} . The resistive value of resistor R_{v1} is controlled by value
19 131, received from counter 130. The bandwidth of op-amp 134 can be further
20 limited by additional capacitance to reduce noise, thereby eliminating the need for
21 a low-pass filter.

22 In a preferred embodiment, variable resistor R_{v1} can be implemented as a
23 series of binary-weighted resistances, each of which is potentially shorted by a
24 corresponding control transistor. The gates of the control transistors can be
25 connected to the individual bit lines of value 131, so that a logical true on any

1 particular bit line causes a corresponding resistance to be included in the series,
2 and a logical false causes the corresponding resistance to be omitted from the
3 series.

4 Both variable resistor R_{v1} and variable gain amplifier 132 can be
5 implemented in a variety of different ways.

6 Optionally, counter 130 has an enable/disable input 135 that enables and
7 disables counter 130. For example, counter 130 may increment or decrement
8 output value 131 when the enable/disable input is logically true, but hold output
9 value 131 constant whenever the enable/disable input is logically false.

10 The enable/disable input allows the gain of amplifier 132 to be set during
11 an initialization period. For example, the enable/disable input may be controlled
12 so that counter 130 is responsive to feedback signal F only during the initialization
13 period. During an operational period following the initialization period,
14 enable/disable input may be set to the disable mode so that digital value 131
15 remains constant. Thus, the gain of amplifier 132 may be set during an
16 initialization period and may remain constant during a subsequent operational
17 period.

18 Utilizing an initialization period to establish a desired amplifier gain is
19 advantageous because the surrounding circuits can be disabled or otherwise
20 configured to generate less noise and interference, thereby producing a more
21 accurate, steady-state evaluation of the proper gain for amplifier 132. Once the
22 proper gain is determined, it can be held steady, which is desirable during actual
23 operation of the integrated circuit. Optionally, the initialization can be repeated at
24 specified intervals to correct for voltage drifts.

Note that although Fig. 2 shows a dedicated feedback receiver, other implementations might utilize an existing data receiver as a feedback component during an initialization period. To accomplish this, data signal D and nominal reference voltage V_{nom} would be multiplexed at an input of a signal receiver. During initialization, the receiver would receive V_{nom} at its input. During normal operation, the receiver would receive the data signal D.

Fig. 4 shows an alternative embodiment that is similar to the embodiment of Fig. 3. As depicted in Fig. 4, driver 114 includes a storage register 150 that is located between counter 130 and variable gain amplifier 132. In this embodiment, control circuits (not shown) may be used to latch value 131 into register 150, from counter 130, after an initialization period. The register provides this latched value, designated in Fig. 4 by reference numeral 151, to variable gain amplifier 132 to control the gain of amplifier 132.

In this embodiment, various control signals, collectively designated by the label "Control" in Fig. 4, are available for use by control circuits within integrated circuit 100 to perform various operations with respect to storage register 150. Such control signals can include a latch signal that latches value 131 into register 150. In addition, the control signals might include data and control signals allowing the value stored by register 150 to be written and read. During a typical initialization or calibration period, register 150 is controlled so that its output 151 duplicates output 131 of counter 130. Once a steady state is reached, register 150 is controlled so that it maintains a constant output 151, regardless of further changes in counter value 131.

An advantage of this configuration is that the value 151 that results from initialization can be read by control circuitry to determine operating parameters of

1 the integrated circuit. Specifically, the control circuitry can determine the adjusted
2 gain of variable amplifier 132 and can potentially use this value to infer other
3 device parameters. Furthermore, register 150 can optionally be written to by
4 control circuits in order to force the gain of amplifier 132 to some predetermined
5 level.

6 The read/write capabilities of register 150 can potentially be used for a
7 variety of functions. For example, by setting value 151 to a wide range of values
8 it is possible to determine the upper and lower limits of V_{comp} that result in correct
9 operation of the device. Specifically, V_{comp} can be lowered (by reducing value
10 151) while testing the circuit at each value, until a value is reached that causes a
11 circuit failure. Subsequently, V_{comp} can be raised (by increasing value 151) until a
12 value is reached that causes a circuit failure. The range of operational V_{comp}
13 values will indicate the available voltage margin of the circuit.

14 As another example, assume that a reference voltage is received from an
15 external source and needs to be somehow translated for use by local circuits. To
16 accomplish this using the circuit of Fig. 4, the external reference voltage is
17 received by amplifier 132 as V_{nom} . During a calibration procedure, a calibrated
18 value 151 is determined that will result in a $V_{dis} = V_{nom}$. This value is read from
19 register 150 and an offset value is added. The resultant value is programmed back
20 into register 150 and used during normal operation of the device, to result in a V_{dis}
21 that is offset from V_{nom} by a desired margin. The desired offset value can be
22 determined at design time and added to the calibrated value 151 after each
23 calibration procedure. Alternatively, the desired offset value can be determined
24 dynamically, as part of an initialization or calibration procedure.
25

1 Fig. 5 shows another embodiment of reference voltage driver 114. This
2 embodiment is similar to the previous embodiments, except that feedback signal F
3 is used to control a charge pump 160. The charge pump is a capacitive device
4 having a control input 162 that receives feedback signal F. Charge pump 160
5 charges a capacitance when feedback signal F is logically true, and discharges a
6 capacitance when feedback signal F is logically false. Charge pump 160 has an
7 analog control voltage output 164 that reflects the voltage of the capacitance. In
8 response to feedback signal F, the control voltage produced at output 164
9 increases when $V_{dis} < V_{nom}$ and decreases when $V_{dis} > V_{nom}$. Output 164 of charge
10 pump 160 is configured to control the gain of reference voltage driver 114. Other
11 types of analog storage devices might be used in place of charge pump 160, such
12 as sample and hold devices.

13 In the embodiment of Fig. 5, variable resistor R_{v2} comprises an analog
14 variable resistor whose resistance is controlled by output 164 of charge pump 160.
15 As an example, the variable resistor might comprise a weighted PMOS adjustable
16 resistor. Similar to the embodiments of Fig. 3 variable resistor variable resistor
17 R_{v2} is configured to control the gain of amplifier 132.

18 Although the embodiments above are described primarily as being used to
19 adjust a distributed reference voltage V_{dis} to be approximately equal to a nominal
20 reference voltage V_{nom} . However, the described techniques can also be used to
21 provide a distributed reference voltage V_{dis} having some non-equal relationship
22 with reference voltage V_{nom} . For example, in the embodiment of Fig. 4 that
23 utilizes a storage register 150, value 151 can be changed in a predefined manner
24 after initialization to offset or translate V_{dis} relative to V_{nom} .

1 The various embodiments described above provide an effective way of
2 establishing a voltage and of compensating or adjusting such a voltage for
3 degradations that might otherwise occur due to factors such as interconnect
4 resistances and device leakage currents. Although the embodiments described
5 above operate with respect to a reference voltage, the same or similar techniques
6 can be used with respect to other types of DC voltages. For example, the
7 described techniques can be used to compensate or adjust supply voltages, ground
8 voltages, and bias voltages.

9 The circuits and techniques described above are particularly useful in
10 integrated circuits, where shrinking geometries have resulted in interconnect traces
11 having increasingly higher impedances. However, the described subject matter
12 can also be used to compensate voltages in other types of circuits, such as voltages
13 distributed between discrete components of PCBs (printed circuit boards) and
14 other circuits.

15 The applicant has found these circuits and techniques to be particularly
16 beneficial in various types of integrated circuit memory and PCB memory circuits,
17 such as dynamic memory devices and boards. Many high-speed memory
18 technologies utilize differential and pseudo-differential signaling techniques, and
19 it is particularly beneficial in these circuits to keep distributed voltages within
20 close tolerances.

21 Although details of specific implementations and embodiments are
22 described above, such details are intended to satisfy statutory disclosure
23 obligations rather than to limit the scope of the following claims. Thus, the
24 invention as defined by the claims is not limited to the specific features described
25 above. Rather, the invention is claimed in any of its forms or modifications that

1 fall within the proper scope of the appended claims, appropriately interpreted in
2 accordance with the doctrine of equivalents.
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